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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/586,908	07/24/2006	Akihiro Goto	1032404-000154	1812

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EXAMINER	
DOAN, NGHIA M	

ART UNIT	PAPER NUMBER
2825	

NOTIFICATION DATE	DELIVERY MODE
07/15/2009	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

ADIPFDD@bipc.com

Office Action Summary	Application No.	Applicant(s)	
	10/586,908	GOTO ET AL.	
	Examiner	Art Unit	
	NGHIA M. DOAN	2825	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *03* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *27 April 2009*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *11-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *11-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. This is response to the Applicant Amendment filed on 04/22/2009. Claims 11-20 remain pending in the instance office action.

Claims 11-13 have been amended.

Claim rejections under 35 U.S.C. 101 and 112 second paragraph have been withdrawn.

Response to Arguments

2. Applicant's arguments with respect to claims 11-13 have been considered but are moot in view of the new ground(s) of rejection.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. **Claims 11-20** are rejected under 35 U.S.C. 103(a) as being unpatentable over Yamazaki et al., (US Pat. 6,617,678) in view of Abe et al., (US Pat. 6,205,636) (see entire document).

5. With respect to **claims 11-20**, Yamazaki teaches a semiconductor device (**claims 11-14**) at least dimensions (e.g. size, shape, position as per **claim 14**) of a semiconductor chip ('678, col. 6, ll. 64-65 as per size and shape, col. 7, ll. 26-45 "chip mounting position" also see fig. 1 and fig. 3, chip [3]) and an interposer ('678, fig. 1 and

fig. 3, relay terminal [5], col. 5, ll. 37-46, different types (e.g. size, shape, position as per **claim 14**)), and bond wire coordinate information (e.g. shape and arrangement position as per **claim 14**) for connecting the semiconductor chip to the interposer (relay terminal) ('678, fig. 1 and fig. 3, connection wiring [6], col. 8, ll. 59-64);

(**claims 11-13 and 15**) the semiconductor chip simulated arrangement data obtained by arranging the semiconductor chip in a position where deviation (offset) (**claim 15**; in-plane or rotation direction ('678, fig. 1, in-plane and/or fig. 3 rotation with angle Θ) in an arrangement position of the semiconductor chip on the interposer is simulated such that the deviation (offset, tolerance) of the semiconductor chip from an original position is simulated ('678, fig. 1, in-plane offset/tolerance/deviation amount [A] and/or fig. 3 rotation with offset/tolerance/deviation amount [B] and angle Θ, col. 7, ll. 26-40 and col. 10, ll. 44-55, and col. 11, ll. 18-26);

(**claims 11-13**) the semiconductor package and the semiconductor chip simulated arrangement data, bond wire simulation data obtained by wiring, using bond wires, the bond wire connection terminals of the semiconductor chip arranged to deviate from an arrangement position in the design data and bond wire connection terminals of the interposer ('678, fig. 1, the offset/tolerance/deviation amount [A], fig. 3, connection (bond) wiring [6] has offset/tolerance/deviation amount [B] and angle Θ, col. 7, ll. 26-40 and col. 10, 44-55 and col. 11, ll. 18-26);

(**claim 13 and 16**) measured clearance between bond/connection wiring (as per **claim 16**) a design rule for the bond wires used for the wiring from the bond wire simulation data ('678, fig. 1, measuring based on the offset/tolerance/deviation amount

[A] and fig. 3, measuring based offset/tolerance/deviation amount [B] and angle Θ, col. 7, ll. 26-40 and col. 10, 44-55 and col. 11, ll. 18-26); and

(**claims 11-13 and 17-18**) a tolerance of fluctuation (offset/deviation) chip and wiring satisfied design rule or wiring rule (as per **17 and 18**) measurement results obtained by the measuring unit ('678, col. 7, ll. 51-56, col. 8, ll. 60-65, col. 9, ll. 7-13).

Yamazaki teach a semiconductor chip arranges with different offset/deviation positions on the interposer (relay terminal), that also causes the connection/bond wiring having different offset/deviation positions with satisfied the design rule (wiring rule) ('678, fig. 1 and fig. 3).

However, Yamazaki does not implicitly teach a design support apparatus for supporting wiring design and storing the output result as recited in **claims 11-13 and 19-20** and does not implicitly outputs analysis results that are used to design the semiconductor package based on the bond wire simulation data and the measurement results.

Abe teaches an automatic assembly apparatus which places a component to the right location based on result of a recognition operation made by an image recognition unit ('636, the abstract, col. 1, ll. 5-10, also see figs. 10, 13 and 17), the apparatus includes input unit/section ('636, fig. 2, [21]), creating unit/section ('636, fig. 2, [37] and fig. 3, [ST6] -[ST7]), measuring unit/section ('636, fig. 2, [35] – [36], fig. 3, [ST8] -[ST9]), analysis unit/section ('636, fig. 2, [43], fig. 3, [ST10]), and (**claims 11-13 and 19-20)** memory/storing unit/section to storing information (chip size/dimension, position/coordination, offset/deviation, ... etc) ('636, fig. 2, [19], fig. 4, [ST11] -[ST13]).

It would have been obvious to one of ordinary skill in the art to use an automatic assembly apparatus disclosed by Abe ('636, the abstract) to support placing a semiconductor chip disclosed by Yamazaki having deviation/offset arrangement on interposer to a correct location that increased operation in advantage ('636, the abstract, col. 1, ll. 5-10, also see figs. 10, 13 and 17; '678, fig. 1 and fig. 3 with descriptions).

Conclusion

6. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. PTO-892.

7. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to NGHIA M. DOAN whose telephone number is (571)272-5973. The examiner can normally be reached on 8:30-5:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jack Chiang can be reached on 571-272-7483. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Nghia M. Doan
/Nghia M Doan/
Examiner, Art Unit 2825

/Thuan Do/
Primary Examiner, Art Unit-2825
07/09/2009